Prototype or Golden Model – what if Formal Methods took the lead in ESL-based design flows?

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This talk discusses the possible role of formal verification techniques in system-level design flows. It is argued that the role of formal verification techniques should not be limited to “bug hunting” alone. Instead, formal technology should assume an entirely new role during the design process. It should be applied in such a way that a formal relationship is provided between an abstract system model and its concrete implementation in RTL hardware or firmware. This will allow for new and highly effective approaches to achieving design goals, such as low power consumption and functional safety. The talk will present several industrial case studies demonstrating the potential of the proposed design methodology.

Short Bio - Wolfgang Kunz

Wolfgang Kunz is professor at the Department of Electrical & Computer Engineering at Technische Universität Kaiserslautern. He conducts research in the area of System-on-Chip design and verification. Currently, his main interest is in formal techniques and their possible role in achieving functional safety and security of embedded systems. Wolfgang Kunz is a Fellow of the IEEE.